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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,507	04/19/2004	Herng-Jer Lee	CFP00353 (20040144.ORI)	3480

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NIKOLAI & MERSEREAU, P.A.
900 SECOND AVENUE SOUTH
SUITE 820
MINNEAPOLIS, MN 55402

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,507	LEE ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-7* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 04/19/2004. Claims 1-7 are pending and presently under examination.

Specification

The abstract of the disclosure is objected to because of minor language informalities. See MPEP § 608.01(b). The Examiner is suggesting the following new attract:

"A method for reordering a scan chain for meeting given constraints and for minimizing peak power dissipation. The given constraints include a maximum peak power dissipation, a maximum scan chain length and a maximum distance between two successive registers. The method further includes embedding a developed tool into an existing VLSI design flow for low-power circuit designs. Furthermore, the characteristics quickly judge if the problem has corresponding feasible solutions and searching the optimal solution. Obtaining modified data, from the given scan chain declaration and the scan pattern data, which satisfy the constraints". Correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation (f), "an event impossibly meeting both the maximum limited distance and the maximum limited distance, and the total length of the scan chain being deleted", which renders the claims indefinite, because it is not clear what is being deleted based on certain required conditions.

Claim 3, the preamble recites the limitation, "wherein an event impossibly meeting both the maximum limited distance is deleted", which renders the claims indefinite, because it is not clear what is being deleted based on certain required conditions.

Claim 4, the preamble recites the limitation, "wherein an event impossibly meeting the maximum of total connection length of scan chain is deleted in the case of", which renders the claims indefinite, because it is not clear what is being deleted based on certain required conditions.

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Hathaway et al. (US Patent No. 6,986,090), filed: February 20, 2002.

Regarding independent Claim 1, Hathaway discloses a method of reordering a scan chain for the design of testability on a chip with low power dissipation as shown in Figure 1, which is a schematic diagram of chip 100 shown before scan chain optimization and chip 110 shown after the scan chain optimization, comprising:

(a) inputting scan chain register circuit data defining the memory elements that are connected to form scan chains on the chip based on their data input and output connections, during circuit placement of designing an integrated circuit semiconductor chip or module. The memory elements of the design are represented by the small squares within chip 100, and the lines interconnecting these squares represent the inter-memory element scan chain connections of an initial scan chain ordering.

(b) inputting test pattern data on the scan chain, as shown in Figure 2.

(c) inputting conditions of the design specification, such as current draw and power consumption of a chip, which are primarily influenced by the amount of switching activity on the chip. During test, the switching activity is usually much larger due to the

nature of the patterns applied. The power consumed during scan operation on average can be reduced by slowing down the rate at which scan cycles are applied, see Background of the Invention. However (col. 8, lines 1-15), Hathaway describes in considering the probabilities that a pair of adjacently connected memory elements will cause a switching event during stimulus scan-in or result scan-out. It is intended that the scan chain be connected such that for most test patterns, the stimulus and result values for most of the adjacently connected memory elements are compatible either with or without intervening inversion in the majority of test patterns. By doing this, one may reduce the switching activity during both stimulus scan-in and result scan-out, and thus reducing power consumption.

(d and e) determining whether a Feasible Solution meeting the maximum limit of distance between two adjacent registers is provided, and creating a database of the two adjacent registers, by altering the effective inter-memory element distances of scan chains. This is achieved by converting the affinity between a pair of memory elements, according to their probability of compatibility, to a number between 1 and a maximum value M, which is then multiplied by the actual distance between the two memory elements and this distance is then used for ordering the scan chains. The value of M represents a trade off between the desire to minimize actual wire lengths and the desire to reduce switching during scan, thus reducing power consumption, (col. 8, lines 16-34).

(f) in view of the 112 Second Paragraph rejection, the Examiner interprets the limitation to correspond deleting the scan chain if the maximum limited distance has not

been met, then go to (step 40), for reordering the scan chains by considering both the memory element placement locations and the compatibility of the memory elements being connected consecutively to form the scan chain.

(g) for the given test pattern (step 10), re-ordering the registers on the scan chain for reduction of power dissipation (step 40), where the scan chains are ordered by considering both the memory element placement locations and the compatibility of the memory elements being connected consecutively to form the scan chain. The goal is to connect consecutively in a scan chain memory elements that are physically in near proximity of each other and that are highly compatible, using well known methods, such as simulated annealing, are advantageously used to determine an ordering meeting the stated goals.

(h) outputting the updated scan chain arrangement and the corresponding scan chain test pattern data, a shown by the Stimulus and Result Patterns.

Regarding Claim 2, Hathaway discloses inputting the memory element and scan input and output coordinates and a set of 20 stimulus and result patterns into the program. The scan-in and scan-out are located around the periphery of the chip, and the memory elements are placed at locations in a 20 by 20 grid representing the chip. The lower left square in the chip is (1, 1), with x and y increasing to the right and up, respectively. Thus, the x and y coordinates of the scan-in and scan-out pins, which are on the periphery of the chip, are all 0 or 21, as shown by the table of the memory element and scan in/out coordinates (Col. 14, lines 38-55).

Regarding Claims 3, 5, 7, Hathaway discloses altering the effective inter-memory element distances of scan chains. This is achieved by converting the affinity between a pair of memory elements, according to their probability of compatibility, to a number between 1 and a maximum value M, which is then multiplied by the actual distance between the two memory elements and this distance is then used for ordering the scan chains. The value of M represents a trade off between the desire to minimize actual wire lengths and the desire to reduce switching during scan, thus reducing power consumption, (col. 8, lines 16-34).

Regarding Claim 6, Hathaway discloses a method of reducing the switching activity during a test scan operation of an integrated circuit (IC) by optimizing the scan design of the IC, by placing consecutively in the scan chain memory elements whose best stimulus value and most likely result value are the same, and those whose best stimulus value and most likely result value are opposite.

Allowable Subject Matter

Claim 4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Teene (US 6272668) Method for cell swapping to improve pre-layout to post-layout timing.
2. Wang et al. (US 20040177299) Scalable scan-path test point insertion technique.
3. Rajski (US 6662327) Method for clustered test pattern generation.
4. Takeoka et al. (US 6282506) Method of designing semiconductor integrated circuit.
5. Caswell et al. (US 20050010832) Method and apparatus of reducing scan power in the process of unloading and restoring processor content by scan chain partition and disable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

U.S. Patent and Trademark Office
401 Dulany Street, RND Bldg.
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

By: 4/14/06

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Office Action: Non-Final Rejection